10/613462 C9C

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent No.:	6,952,115 B1
Issued:	October 4, 2005
First Named Inventor:	William B. Andrews
Title	PROGRAMMABLE I/O INTERFACE FOR FPGAS AND OTHER PLDS

REQUEST FOR EXPEDITED ISSUANCE OF CERTIFICATE OF CORRECTION PURSUANT TO 37 CFR 1.322

Certificate of Corrections Branch
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Review of the above-identified patent has revealed errors in the patent attributable solely to the Patent and Trademark Office. Applicants therefore request that a Certificate Of Correction be issued to correct these errors.

The location of the errors in the patent and the corresponding correct language in the application file are set forth below:

Error in Patent	Correct Language in Application File
Col. 18, line 10 (claim 1)	Amendment filed 2/18/05, claim 1, line 17

Documentation supporting this request and a form PTO/SB/44 showing the corrections are enclosed.

Although no fees are believed due, the Commissioner is hereby authorized to charge any fees associated with this communication to Deposit Account No. 501958.

Respectfully submitted,

Date: 11/18/05

By: _____

Mark L Becker
Associate General Counsel, IP
Reg. No. 31,325
Customer No. 29416

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contains bits b and d. After a time-domain transfer implemented by clocking the two half-rate data signals through FF18 and FF19, respectively, the resulting data signals correspond to two demultiplexed DDR data signals provided on signal lines INSHP0 and INSHP1, thereby completing the (1×2) data demux input mode.

Those skilled in the art will understand how to extend the exemplary processing represented in FIG. **8** to the other input modes of operation supported by the circuitry of FIG. **3**.

Alternative Implementations

Depending on the particular implementation, the architectures shown in FIGS. **3** and **5** may share certain components. For example, in a preferred implementation, update generator **310** of FIG. **3** and update generator **502** of FIG. **5** are implemented as a single, shared update generator. Similarly, control signal LSR and the clock signals SC and EC are shared.

The present invention has been described in the context of a particular architecture that can support multiplexing modes up to (4:1) and demultiplexing modes up to (1:4), without or without corresponding SDR/DDR conversion. As suggested previously, the present invention is not so limited. Higher levels of multiplexing and demultiplexing can be achieved by adding additional flip-flops to appropriate stages in the designs and providing appropriate control signals to exploit the functionality of such additional components.

The present invention has been described in the context of circuitry that is driven by a single system clock and a single edge clock. Those skilled in the art will understand that the present invention can be expanded to employ more than two clocks with appropriate muxing to select specific clocks to be used to drive particular components.

Although the present invention has been described in the context of FPGAs, those skilled in the art will understand that the present invention can be implemented in the context of other types of PLDs, such as, without limitation, mask-programmable gate arrays (MPGAs), SRAM-based PLDs, DRAM-based PLDs, flash memory-based PLDs, and ASICs with user control signals.

It will be further understood that various changes in the details, materials, and arrangements of the parts which have been described and illustrated in order to explain the nature of this invention may be made by those skilled in the art without departing from the scope of the invention as expressed in the following claims.

What is claimed is:

1. A programmable logic device (PLD), comprising a logic core connected to an input/output (I/O) interface, the I/O interface comprising one or more programmable I/O buffers (PIBs), wherein:

at least one PIB can be programmed to perform three or more of:

(a) a double data rate (DDR) input mode in which an incoming DDR data signal is converted into two single data rate (SDR) data signals that are made available to the logic core;

(b) one or more demux input modes, different from the DDR input mode, in which an incoming data signal is demultiplexed into two or more lower-rate data signals that are made available to the logic core;

(c) one or more DDR demux input modes in which an incoming DDR data signal is converted into four or more lower-rate SDR data signals that are made available to the logic core; and

(d) one or more additional input modes in which an incoming data signal is made available to the logic core without any demultiplexing or DDR-to-SDR conversion; and the at least one PIB can be programmed to perform three or more of:

(a) a DDR output mode in which two SDR data signals from the logic core are converted into a single outgoing DDR data signal;

(b) one or more mux output modes, different from the DDR output mode in which two or more data signals from the logic core are multiplexed into a single, higher-rate, outgoing data signal;

(c) one or more DDR mux output modes in which four or more SDR data signals from the logic core are converted into a single, higher-rate, outgoing DDR data signal; and

(d) one or more additional output modes in which a data signal from the logic core is provided as an outgoing data signal without any multiplexing or SDR-to-DDR conversion.

2. The invention of claim **1**, wherein the PLD is a field programmable gate array (FPGA).

3. The invention of claim **1**, wherein:

the one or more additional input modes comprise a pass-through data input mode and an input register mode; and

the one or more additional output modes comprise a pass-through data output mode and an output register mode.

4. The invention of claim **1**, wherein, during each DDR demux input mode:

the incoming DDR data signal is converted into first and second SDR data signals;

the first SDR data signal is demultiplexed into a first set of two or more lower-rate SDR data signals; and

the second SDR data signal is demultiplexed into a second set of two or more lower-rate SDR data signals.

5. The invention of claim **1**, wherein, during each DDR mux output mode:

a first set of two or more SDR data signals are multiplexed into a first higher-rate SDR data signal;

a second set of two or more SDR data signals are multiplexed into a second higher-rate SDR data signal; and

the first and second SDR data signals are converted into the outgoing DDR data signal.

6. The invention of claim **1**, wherein the PIB supports a plurality of different demux input modes having different levels of demuxing, a plurality of different DDR demux input modes having different levels of demuxing, a plurality of different mux output modes having different levels of muxing, and a plurality of different DDR mux output modes having different levels of muxing.

7. The invention of claim **6**, wherein:

the plurality of demux input modes includes (1:1), (1:2), and (1:4) levels of demuxing;

the plurality of DDR demux input modes includes (1:1), (1:2), and (1:4) levels of demuxing, each combined with DDR-to-SDR conversion;

the plurality of mux output modes includes (1:1), (2:1), and (4:1) levels of muxing; and

the plurality of DDR mux output modes includes (1:1), (2:1), and (4:1) levels of muxing, each combined with SDR-to-DDR conversion.

8. The invention of claim **1**, wherein, to support the input modes, the PIB comprises:

PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission: 9

Application Number	10/613,462
Filing Date	7/3/2004
First Named Inventor	William B Andrews
Art Unit	2819
Examiner Name	Daniel D Chang
Attorney Docket Number	1054.025

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
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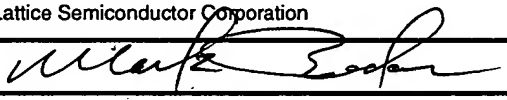
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please Identify below):
  Request for Certificate of Correction

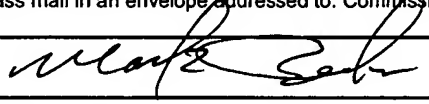
Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Lattice Semiconductor Corporation		
Signature			
Printed name	Mark L Becker		
Date	11/18/05	Reg. No.	31325

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature			
Typed or printed name	Mark L Becker	Date	11/18/05

PTO/SB/80 (04-05)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☑ Practitioners associated with the Customer Number: 29416

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☑ The address associated with Customer Number: 29416

OR

☐ Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address:

Lattice Semiconductor Corporation
5555 NE Moore Court
Hillsboro, OR 971247-6421

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	Martin R. Baker	Date	June 30, 2005
Name	Martin R. Baker	Telephone	503-268-8000
Title	Vice President & General Counsel		

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/96 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Andrews et al.

Application No./Patent No.: 6,952,115 Filed/Issue Date: 10/4/2005

Entitled: PROGRAMMABLE I/O INTERFACES FOR FPGAS AND OTHER PLDS

Lattice Semiconductor Corporation, a corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. [x] the assignee of the entire right, title, and interest; or

2. [ ] an assignee of less than the entire right, title and interest.
The extent (by percentage) of its ownership interest is_____ %

in the patent application/patent identified above by virtue of either:

A. [x] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 014269, Frame 0191, or for which a copy thereof is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as shown below:

1. From:_____ To:_____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From:_____ To:_____
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[ ] Additional documents in the chain of title are listed on a supplemental sheet.

[ ] Copies of assignments or other documents in the chain of title are attached.
[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Mark L Becker — 11/18/05
Signature — Date

Mark L Becker — 503-268-8629
Printed or Typed Name — Telephone Number

Associate General Counsel, IP
Title

PTO/SB/44 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,952,115 B1

APPLICATION NO.: 10/613,462

ISSUE DATE : October 4, 2005

INVENTOR(S) : Andrews et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 18, line 10: "output mode in which" should read -- output mode, in which --.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Lattice Semiconductor Corporation
5555 NE Moore Ct., Hillsboro, OR 97124

CUSTOMER NO. 22186 *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re: Attorney Docket No. 1054.025

In re application of: William B. Andrews, Fulong Zhang, and Harold Scholz

Serial No.:	10/613,462	Group Art Unit:	2819
Filed:	07/03/03	Examiner:	Daniel Chang
Matter No.:	L03-03	Phone No.:	571-272-1801

For: Programmable I/O Interfaces for FPGAs and Other PLDs

AMENDMENT UNDER 37 CFR 1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Amendment is filed in response to the office action of 12/10/04.

* * * * *

Certification Under 37 CFR 1.8

Date of Deposit February 18, 2005.

I hereby certify that this correspondence is being deposited in the United States Postal Service with sufficient postage as first class mail under 37 CFR 1.8 on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

MARY E. CANIZ
(Name of person mailing)

Mary E. Caniz
(Signature of person mailing)

CLAIMS

1. (currently amended) A programmable logic device (PLD), comprising a logic core connected to an input/output (I/O) interface, the I/O interface comprising one or more programmable I/O buffers (PIBs), wherein:

at least one PIB can be programmed to perform ~~two~~ three or more of:

(a) a double data rate (DDR) input mode in which an incoming DDR data signal is converted into two single data rate (SDR) data signals that are made available to the logic core;

(b) one or more demux input modes, different from the DDR input mode, in which an incoming data signal is demultiplexed into two or more lower-rate data signals that are made available to the logic core;

(c) one or more DDR demux input modes in which an incoming DDR data signal is converted into four or more lower-rate SDR data signals that are made available to the logic core; and

(d) one or more additional input modes in which an incoming data signal is made available to the logic core without any demultiplexing or DDR-to-SDR conversion; and

the at least one PIB can be programmed to perform ~~two~~ three or more of:

(a) a DDR output mode in which two SDR data signals from the logic core are converted into a single outgoing DDR data signal;

(b) one or more mux output modes, different from the DDR output mode, in which two or more data signals from the logic core are multiplexed into a single, higher-rate, outgoing data signal;

(c) one or more DDR mux output modes in which four or more SDR data signals from the logic core are converted into a single, higher-rate, outgoing DDR data signal; and

(d) one or more additional output modes in which a data signal from the logic core is provided as an outgoing data signal without any multiplexing or SDR-to-DDR conversion.

2. (original) The invention of claim 1, wherein the PLD is a field programmable gate array (FPGA).

3. (original) The invention of claim 1, wherein:

the one or more additional input modes comprise a pass-through data input mode and an input register mode; and

the one or more additional output modes comprise a pass-through data output mode and an output register mode.

4. (original) The invention of claim 1, wherein, during each DDR demux input mode:

the incoming DDR data signal is converted into first and second SDR data signals;

the first SDR data signal is demultiplexed into a first set of two or more lower-rate SDR data signals; and

the second SDR data signal is demultiplexed into a second set of two or more lower-rate SDR data signals.

5. (original) The invention of claim 1, wherein, during each DDR mux output mode:

a first set of two or more SDR data signals are multiplexed into a first higher-rate SDR data signal;

a second set of two or more SDR data signals are multiplexed into a second higher-rate SDR data signal; and

the first and second SDR data signals are converted into the outgoing DDR data signal.